SMD1210 Series

Features
- Surface Mount Devices
- Lead free device
- Surface Mount packaging for automated assembly
- Agency recognition: UL

Applications
Almost anywhere there is a low voltage power supply, up to 30V and a load to be protected, including:
- Computer mother board, Modem. USB hub
- PDAs & Charger, Analog & digital line card
- Digital cameras, Disk drivers, CD-ROMs,

Sea & Land

Performance Specification

Model	Marking	V_{max} (Vdc)	I_{max} (A)	I_{hold} @25℃ (A)	I_{trip} @25℃ (A)	P_d Max. (W)	Maximum Time To Trip		Resistance	
							Current (A)	Time (Sec)	Ri_{min} (Ω)	R1max (Ω)
SMD1210-005	αA	30.0	100	0.05	0.15	0.6	0.3	1.50	2.800	50.000
SMD1210-010	αB	30.0	100	0.10	0.30	0.6	0.5	0.60	0.800	15.000
SMD1210-020	αC	30.0	100	0.20	0.40	0.6	8.0	0.02	0.400	5.000
SMD1210-035	αD	6.0	100	0.35	0.75	0.6	8.0	0.20	0.200	1.300
SMD1210-050	αF	13.2	100	0.50	1.00	0.6	8.0	0.10	0.180	0.900
SMD1210-075	αG	6.0	100	0.75	1.50	0.6	8.0	0.10	0.070	0.400
SMD1210-110	αH	6.0	100	1.10	2.20	0.6	8.0	0.30	0.050	0.210
SMD1210-150	αL	6.0	100	1.50	3.00	0.6	8.0	0.50	0.030	0.110

Ihold = Hold Current. Maximum current device will not trip in 25℃ still air.
Itrip = Trip Current. Minimum current at which the device will always trip in 25℃ still air.
Vmax = Maximum operating voltage device can withstand without damage at rated current (Imax).
Imax = Maximum fault current device can withstand without damage at rated voltage (Vmax).
Pd = Maximum power dissipation when device is in the tripped state in 25℃ still air environment at rated voltage.
Rimin/max = Minimum/Maximum device resistance prior to tripping at 25℃.
$R1_{max}$ = Maximum device resistance is measured one hour post reflow.
CAUTION : Operation beyond the specified ratings may result in damage and possible arcing and flame.

Environmental Specifications

Test	Conditions	Resistance change
Passive aging	+85℃, 1000 hrs.	±5% typical
Humidity aging	+85℃, 85% R.H. , 168 hours	±5% typical
Thermal shock	+85℃ to -40℃, 20 times	±33% typical
Resistance to solvent	MIL-STD-202,Method 215	No change
Vibration	MIL-STD-202,Method 201	No change
Ambient operating conditions : - 40 ℃ to 85 ℃		
Maximum surface temperature of the device in the tripped state is 125 ℃		

AGENCY APPROVALS : U.L pending

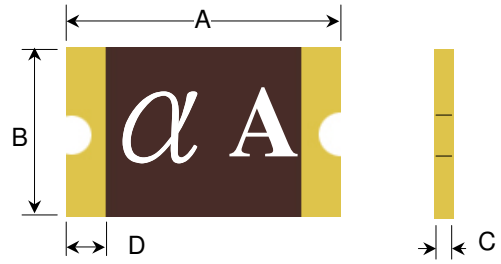
I_{hold} versus temperature

Model	Maximum ambient operating temperature (Tmao) vs. hold current (Ihold)								
	-40℃	-20℃	0℃	25℃	40℃	50℃	60℃	70℃	85℃
SMD1210-005	0.08	0.07	0.06	0.05	0.04	0.04	0.03	0.03	0.02
SMD1210-010	0.16	0.14	0.12	0.10	0.08	0.07	0.06	0.05	0.03
SMD1210-020	0.29	0.26	0.22	0.20	0.16	0.14	0.13	0.11	0.08
SMD1210-035	0.47	0.45	0.40	0.35	0.33	0.28	0.24	0.21	0.18
SMD1210-050	0.76	0.67	0.58	0.50	0.43	0.40	0.36	0.32	0.28
SMD1210-075	1.00	0.97	0.86	0.75	0.64	0.59	0.54	0.48	0.40
SMD1210-110	1.69	1.48	1.29	1.10	0.88	0.76	0.65	0.57	0.43
SMD1210-150	2.13	1.92	1.71	1.50	1.26	1.14	1.01	0.89	0.71

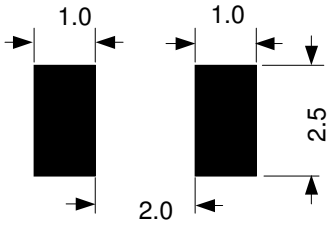
Construction and Dimension (Unit:mm)

Model	A		B		C		D
	Min.	Max.	Min.	Max.	Min.	Max.	Min.
SMD1210-005	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-010	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-020	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-035	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-050	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-075	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-110	3.00	3.43	2.35	2.80	0.30	0.80	0.30
SMD1210-150	3.00	3.43	2.35	2.80	0.60	1.40	0.30

Dimensions & Marking



Recommended pad layout (mm)



Termination pad characteristics

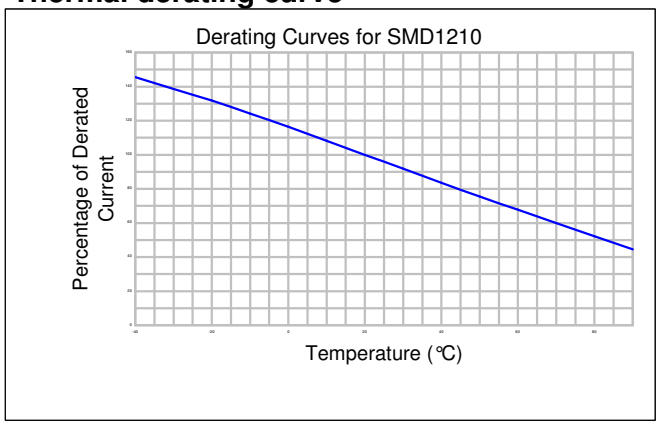
Terminal pad materials： Tin-Plated Nickle-Copper or Gold-Plated Nickle-Copper

Terminal pad solderability： Meets EIA specification RS186-9E and ANSI/J-STD-002 Category 3.

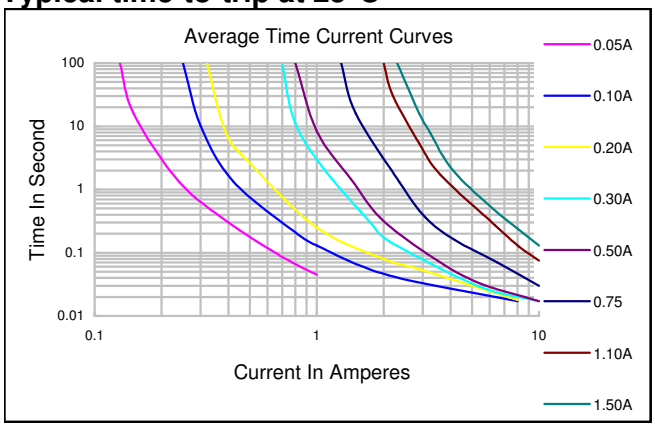
Rework

Use standard industry practices, the removal device must be replaced with a fresh one.

Thermal derating curve



Typical time-to-trip at 25℃



WARNING:

· Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
· PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
· Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
· Use PPTC with a large inductance in circuit will generate a circuit voltage (L di/dt) above the rated voltage of the PPTC.
· Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
· Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
· Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.